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October 12, 2000

BOX PATENT APPLICATION  
Assistant Commissioner for Patents  
Washington, D.C. 20231

Re: Toshiyuki ODA  
CDMA RECEIVER AGC CIRCUIT AND CDMA DEMODULATOR  
Our Ref. Q61276

Dear Sir:

Attached hereto is the application identified above including 23 sheets of the specification, claims, 5 sheets of formal drawings, executed Assignment and PTO 1595 form, and executed Declaration and Power of Attorney. Also enclosed is the Information Disclosure Statement with form PTO-1449 and references.

The Government filing fee is calculated as follows:

Total claims	9	-	20	=		x	\$18.00	=	\$0.00
Independent claims	6	-	3	=	3	x	\$80.00	=	\$240.00
Base Fee									\$710.00
Multiple Dependent Claim Fee									\$270.00

<b>TOTAL FILING FEE</b>	<b>\$1220.00</b>
Recordation of Assignment	\$40.00
<b>TOTAL FEE</b>	<b>\$1260.00</b>

Checks for the statutory filing fee of \$1220.00 and Assignment recordation fee of \$40.00 are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from October 13, 1999 based on Japanese Application No. 290925/1999. The priority document is enclosed herewith.

Respectfully submitted,  
SUGHRUE, MION, ZINN,  
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10/12/00

CDMA RECEIVER AGC CIRCUIT AND CDMA DEMODULATOR

BACKGROUND OF THE INVENTION

The present invention relates to an AGC (Automatic Gain Control) circuits in CDMA (Code Division Multiple Access) receivers.

As is well known in the art, the CDMA system is one of multiple access system techniques adopted in cellular systems (or mobile communication systems) such as car telephone systems and portable telephone systems, in which communication is performed simultaneously by a plurality of stations in the same frequency band. Well known as other multiple access techniques than the CDMA system are FDMA (Frequency Division Multiple Access) system and TDMA (Time Division Multiple Access) system. Over these other multiple access system techniques, the CDMA system has an advantage in higher frequency utilization efficiency and more user accommodation.

In the CDMA system, the spectrum of data signal to be transmitted is spread in a band sufficiently wide compared to the intrinsic data bandwidth, so that multiple connection is performed by spread spectrum communication.

The cellular system (or mobile communication system) generally includes mobile communication terminals (hereinafter referred to as "mobile stations") MS and a plurality of base stations BS servicing cells. The CDMA system is employed as the third generation Mobile communication system. As

hand-over in the case of cross-passing of a CDMA system mobile station MS from one cell to another, soft hand-over is executed, in which radio wave signal from the base station BS before the cross-passing and radio wave signal from the base station MS after the cross-passing are combined.

In such CDMA system, for increasing the subscriber's capacity a power control system is adopted, in which the SIR (signal-to-interference ratio) of receiver input is controlled to be constant. By the term "SIR" is meant the ratio of the level of desired wave received signal power to the level of interference signal power received by the pertinent user from a different user.

As power control system, Japanese Patent No. 2855173 (hereinafter referred to as Prior Art 1) proposes a "CDMA demodulating system", in which the level of received power of pass after despreading is obtained by inserting a pilot signal of a known pattern in signal intermittently at a predetermined cycle frequency.

As further prior art techniques pertaining to the present invention, the following techniques are well known in the art. Japanese Patent Laid-Open No. 9-275361 (hereinafter referred to Prior Art 2) discloses receiver and transmitter, in which waveform distortion of even modulated waves having data in the amplitude is eliminated by instantly forming an AGC loop. In the receiver disclosed in Prior Art 2, a power amplifier

amplifies a received signal by an antenna. A variable gain attenuator attenuates the gain of the received signal based on a holder circuit output voltage. A first mixer and a first local oscillator operate together to convert the output signal from the variable gain attenuator to an intermediate frequency signal, and a first band-pass filter limits the band of the intermediate frequency signal. A second local oscillator and a second mixer operate together for further frequency conversion of the first band-pass filter output, and a second band-pass filter limits the band. A limit amplifier limit-amplifies the second band-pass filter output signal, and its out-put is fed to a detector for detection. A comparator obtains a difference voltage between the detector output voltage and a reference voltage. When the difference voltage becomes positive, a timing generator generates a timing signal. Under control of the timing signal, the holder circuit holds the comparator output signal, and the variable gain attenuator attenuates the gain of the received signal based on the holder circuit output signal. A time constant circuit integrates the detector output, and an adder adds together the outputs of the time constant circuit and the holder circuit.

Japanese Patent Laid-Open No. 10-224297 (hereinafter referred to as Prior Art 3) discloses mobile station transmission power level control method and mobile communication system. Prior Art 3 concerns a

problem in the prior art. Specifically, in the prior art mobile station transmission power level control, which is performed by a base station, is realized by step-wise control of control amount, which is fixed for each time slot. However, sometimes a long time is taken until the power level is converged to a predetermined level. In Prior Art 3, it is sought to prevent failure of convergence in a communication time particularly in burst communication. Specifically, the power level control executed in the first time slot from the start of communication is performed based on softly changing control amount, while the power level control in the second and following time slot is performed step-wise based on a fixed control amount.

Japanese Patent Disclosure No. 8-2058 (hereinafter referred to as Prior Art 4) discloses an AGC (automatic gain control) system, which is suited for fast and stable AGC in fading circumstances as in mobile communication, when applied to a direct conversion system a time division transmitting/receiving switching system. In Prior Art 3, the signal power level in burst section is detected by making use of a timing signal for time division transmission and reception, and gain control in the next reception time slot is performed based on the detection output. A gain control voltage is set at the start of received burst, and DC off-set can be removed by short-circuiting (or clamping) by short-circuiting the output of a DC block circuit capacitor to ground in a

state that any received signal has not yet arrived. It is thus possible to completely remove the advantages of DC off-set variation due to AGC and improve the AGC speed.

However, Prior Art 1 has no mention about the  
5 control timing. Depending on the radio wave propagation circumstances, the line quality may be deteriorated by inadequate control timing, and in an extreme case the line may be broken.

Now, inconvenience which may be encountered when  
10 the control timing is inadequate will be described with reference to Figs. 5(a) and 5(b).

It is important to control the control timing. Specifically, the result of calculation of average power level is desirably fed back from an instant corresponding  
15 to the forefront of the next slot.

In Fig. 5(a), two successive slots are shown. The first slot is referred to as slot 1, and the next slot is referred to slot 2. A predetermined period of time from the slot forefront is used for power level  
20 calculation. In the control shown in Fig. 5(a), the calculated power level in slot 1 is less than a desired level, and it is thus updated to the desired level from the instant corresponding to the forefront of slot 2. This control is ideal. However, such control is actually  
25 impossible.

Actually, as shown in Fig. 5(b), the control involves rising time. Accordingly, by taking the rise time into considerations the control is started at an

instant earlier than the forefront of slot 2 with an aim of obtaining coincidence of the instant of reaching of a desired voltage with the forefront of slot 2. Control of signal 1 in Fig. 5(b) corresponds to this case.

5       The control is not started at an indiscriminately earlier instant for the following reason. The transmitting side transmits slots at a constant power level. Therefore, a change in the level of power inputted to the demodulator during a slot results in  
10 generation in an demodulation error or like undesired result. It is thus intended to minimize control change during the slot. This is the reason for the above.

          However, the amount of control change (i.e., amount of correction) is not fixed. Now, inconvenience which  
15 may be encountered unless the control timing is changed will be described.

          As an example, a propagation channel having a characteristic close to static characteristic with less fading effects will be considered. In this case, the  
20 time-wise change in the error of power level from desired level, i.e., the control amount, is not so much. Therefore, feed-back is provided at an instant earlier than desired instant. Waste is thus involved from the standpoint of minimizing the change in power level with  
25 time in one slot.

          Now, a propagation channel with fading present therein will be considered. In this case, the received power level change with time may be great, i.e., the

control amount may be extremely great. Therefore, feed-back is provided later than the desired instant. With this delay from the desired instant, the forefront of the slot used for the power level calculation occurs during the rise of voltage, thus disabling correct calculation. Signal 2 in Fig. 5(b) corresponds to this case.

What is shown above is the inconvenience encountered in the case of failure of adequate control of the control timing. Furthermore, in the case of using a known pilot signal for the power level calculation, the pilot signal may be too short to obtain correct average power level calculation.

Prior Art 2 shows an invention concerning a gain attenuator control circuit provided in a TDMA radio system, and it is thus set apart from the circuit applied to the CDMA system according to the present invention. Although according to Prior Art 2 a timing signal is generated, it is a signal synchronized to a received slot in the case where received signal peculiar to the TDMA system is a burst signal. That is, the timing signal disclosed in Prior Art 2 is quite irrelevant to the timing control of control amount, which is important according to the present invention.

According to Prior Art 3, time required from the start of transmission by a mobile station till convergence of the transmitted signal power level control is reduced by the power level control based on

softly changing control amount in the first time slot from the start of communication. Specifically, In Prior Art 3 base station transmits transmission signal power level control signal of variable control amount to mobile station, and the mobile station controls the transmitted signal power level control in response to the transmitted signal power level control signal. That is, what is disclosed is merely reverse link power level control. Prior art 3 thus is essentially set apart from the control according to the present invention, in which the gain of signal received in own station is controlled to make the received signal power level constant.

According to Prior art 4, although the AGC system is disclosed, like the above Prior Art 2 the communication system as subject is a time division transmission/reception communication system, which is set apart from the CDMA system as the subject of the present invention. Although Prior Art 4 shows the use of timing signal, this signal is for time division transmission and reception, and gain control in the next time slot is performed based on an output obtained by burst section signal power level detection. Thus, the timing signal disclosed in Prior Art 4, like the above Prior Art 2, is quite irrelevant to the control timing of control amount as concerned by the present invention.

## SUMMARY OF THE INVENTION

An object of the present invention, accordingly, is to provide a CDMA receiver AGC circuit (i.e., CDMA

demodulator), which permits adequately controlling the control timing.

According to a first aspect of the present invention, there is provided an AGC circuit in a CDMA receiver comprising an AGC loop for calculating received signal power level from a received signal and controlling the received signal power level to be constant, wherein the AGC loop includes means for controlling the control timing based on control amount.

According to a second aspect of the present invention, there is provided a CDMA demodulator for receiving and demodulating a spread spectrum signal comprising an AGC loop including an intermediate frequency signal converter for converting the spread spectrum signal to an intermediate frequency signal and an AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage, wherein the AGC loop includes a power level calculating unit for calculating the level of full power in the band of a channel under reception.

The power level calculating unit starts the power level calculation from an instant corresponding to the forefront of a slot. The power level calculating unit makes the length of the subject of calculation to be variable. The AGC loop further includes a control unit for calculating control time according to the result of calculation in the power level calculating unit, calculating and controlling the control timing based on

control amount and feeding out the control voltage. The power level calculating unit starts the power level calculation from an intermediate part of slot.

According to a third aspect of the present

5 invention, there is provided a CDMA demodulator for receiving and demodulating a spread spectrum signal comprising: an intermediate frequency signal converter for receiving the spread spectrum signal and converting the same signal to an intermediate frequency signal; an

10 AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage;

a demodulating unit for demodulating the output signal of the AGC amplifier to a base-band signal; a first low-pass filter for limiting the band of the base-band  
15 signal to a band corresponding to one channel and feeding out a first low-pass filter output signal; an A/D converter for quantizing the level of full power in the band of the first low-pass filter output signal and feeding out the quantized signal; a power level

20 calculating unit for averaging the power level of the quantized signal for a predetermined period of time from an instant corresponding to the forefront of slot and feeding out an average power level signal representing the average power level; a control unit for calculating  
25 control time based on the average power level represented by the average power level signal and feeding out control data upon reaching of a predetermined instant of time; an A/D converter for converting the control data to an

analog control signal; and a second low-pass filter for waveform shaping the along control signal and feeding the control voltage to the AGC amplifier.

According to a fourth aspect of the present invention, there is provided a control timing controlling method adopted in an AGC circuit in a CDMA receiver comprising an AGC loop for computing a received signal power level from a received signal and controlling the received signal power level to be constant, wherein by taking the rise time of the next slot, the instant of start of control is variably set to be earlier than the forefront of the next slot so as to obtain coincidence of the instant of reaching of a desired voltage with the forefront of the next slot.

In the present invention, the control timing is changed based on the control amount, and it is thus possible to obtain stable reception quality. In addition, by causing power level calculation from an instant corresponding to an intermediate part of slot, it is possible to prevent erroneous power level measurement due to voltage rise shortage.

Other objects and features will be clarified from the following description with reference to attached drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a CDMA receiver AGC circuit according to an aspect of the present invention;

Figs. 2(a) and 2(b) are timing charts of control

timing which is variable based on the control amount in Fig. 1;

Fig. 3 is a flow chart for the operation of the CDMA demodulator in CDMA receiver AGC circuit if Fig. 1;

5 Figs. 4(a) and 4(b) are timing charts showing an example in which the power calculation of the present invention is executed during the slot; and

Figs. 5(a) and 5(b) are timing charts showing the fixed control timing for the control amount.

#### 10 PREFERRED EMBODIMENTS OF THE INVENTION

Preferred embodiments of the present invention will now be described with reference to the drawings.

An embodiment of the CDMA receiver AGC circuit (or CDMA modulator) according to the present invention will  
15 now be described with reference to Fig. 1. The illustrated CDMA receiver AGC circuit (or CDMA demodulator) comprises a transmitting/receiving antenna (hereinafter referred to merely as antenna) 11, an IF signal converter 12, an AGC (automatic gain control)  
20 amplifier 13, a demodulator 14, a first LPF (low-pass filter) 15, an A/D (analog-to-digital) converter 16, a power level calculator 17, a control unit 18, a D/A (digital-to-analog) converter 19, a second LPF (low-pass filter) 20 and a despreading unit 21.

25 The antenna 11 is connected to the IF converter 12. The IF signal converter 12 is connected to the AGC amplifier 13. The AGC amplifier 13 is connected to the demodulator 14. The demodulator 14 is connected to the

first LPF 15. The first LPF 15 is connected to the A/D converter 16. The A/D converter 16 is connected to the power level calculator 17. The power level calculator 17 is connected to the control unit 18 and also to the  
5 despreading unit 21. The control unit 18 is connected to the D/A converter 19. The D/A converter 19 is connected to the second LPF 20. The second LPF 20 is connected to the AGC amplifier 13.

The AGC amplifier 13, the demodulator 14, the first  
10 LPF 15, the A/D converter 16, the power level calculator 17, the control unit 18, the D/A converter 19 and the second LPF 20 together constitute an AGC loop.

As spread spectrum signal (i.e., CDMA signal) received by the antennas 12 passes through the IF signal  
15 converter 12 to obtain an IF (intermediate frequency) signal. That is, the IF signal converter 12 converts the spread spectrum signal to the IF signal. The IF signal is amplified in the AGC amplifier 13, the gain of which is variable, with a control voltage to be described later,  
20 and then demodulated in the demodulator 14 to a base-band signal. That is, the AGC amplifier 13 amplifies the IF signal in response to the control voltage to feed out an AGC output signal, and the demodulator 14 demodulates the AGC signal to generate the base-band signal.

25 The first LPF 15 limits the band of the base-band signal to a band corresponding to one channel. The A/D converter 16 quantizes the full power in this band. The power level calculator 17 averages the power level for

5 a given period of time from the forefront of slot, and feeds out the result to the control unit 18. More specifically, the first LPF 15 passes only low frequency components of the base-band signal to feed out a first LPF output signal. The A/D converter 16 quantizes the full power of the first LPF output signal, and feeds out a quantized signal (as digital signal). The power level calculator 17 averages the quantized signal power level for a given period of time from the forefront of slot, and feeds out an average power level signal representing the average power level to the control unit 18.

10 The control unit 18 calculates control time, and upon reaching of a predetermined time instant, it feeds out control data to the D/A converter 18. More specifically, the control unit 19 calculates the control time based on the average power level represented by the average power level signal, and feeds out the control data, which represents control amount, to the D/A converter 19 at a timing (or time instant) corresponding to the control amount. The D/A converter 19 converts the control data to an analog control signal. The second LPF 20 waveform shapes the output (i.e., analog control signal) of the D/A converter 19, and feeds out the control voltage to the AGC amplifier 13. More specifically, the second LPF 20 passes only low frequency components of the analog control signal, and feeds out a second LPF output signal as control voltage to the AGC amplifier 13.

Slot forefront data is fed out from the despreading unit 21 to the power level calculator 17.

The control timing according to the present invention will now be described with reference to Fig.

- 5 2. As noted before, it is important to control the control timing. Specifically, the result of calculation of average power level is desirably fed back from an instant corresponding to the forefront of the next slot.

In Fig. 2(a), two successive slots are shown.

- 10 These slots are the same as those shown in Fig. 5(a). Again the first slot is referred to as slot 1, and the next slot is referred to as slot 2. The power level calculating unit 17 uses a predetermined period of time for power level calculation. In the control shown in Fig. 15 2(a), the calculated power level in slot 1 is less than a desired level, and it is thus updated to the desired level from the instant corresponding to the forefront of slot 2. This control is ideal. However, such control is actually impossible.

- 20 Actually, as shown in Fig. 2(b), the control involves rising time. Accordingly, by taking the rise time into considerations, the control is started at an instant earlier than the forefront of slot 2 with an aim of obtaining coincidence of the instant of reaching of 25 a desired voltage with the forefront of slot 2. Control of signal 1 in Fig. 2(b) corresponds to this case.

The control is not started at an indiscriminately earlier instant for the following reason. The

transmitting side transmits slots at a constant power level. Therefore, a change in the level of power inputted to the demodulator during a slot results in generation of a demodulation error or like undesired  
5 result. It is thus intended to minimize control change during the slot. This is the reason for the above.

However, the sum of control change (i.e., amount of correction) is not fixed. Therefore, unless the control timing is changed, the slot forefront used for  
10 the power level calculation occurs during the voltage rise as in the case of above signal 2 in Fig. 5(b). In this case, correct calculation can no longer be obtained.

In contrast, according to the present invention the control timing is changed based on the control amount  
15 as shown in Fig. 2(b). It is thus possible to provide feed-back always at the same timing (in this example at the forefront of slot).

The operation of the CDMA demodulator shown in Fig. 1 will now be described with reference to Fig. 3.

20 The power level calculating unit 17 adds together power for a predetermined period of time (step S1), and then calculates the average power level (step S2). The power level calculation unit 17 thus feeds out an average power level signal representing the average power level  
25 to the control unit 18. The control unit 18 calculates control timing based on the average power level (step S3). Then, the control unit 18 waits for a predetermined wait time (step S4), and then starts control by feeding

out control data to the D/A converter 19 (step S5).  
Subsequently after the lapse of the sum of a time  
necessary for the rise of voltage in the AGC amplifier  
13 and the demodulator 14 and a time necessary for the  
5 rise of voltage in the first LPF 1 (step S6), the desired  
voltage is reached by the output of the first LPF 15 (step  
S7).

The embodiment as described above is by no means  
limitative, and can be variously changed and modified  
10 without departing from the scope of the present invention.  
For example, while in the above embodiment the power level  
calculating unit 17 starts the power level calculation  
from the forefront of slot as shown in Fig. 2(a), the  
calculation may also be started from an intermediate part  
15 of slot as shown in Fig. 4(a). By so doing, it is possible  
to prevent erroneous power level measurement due to  
voltage rise shortage.

As has been described in the foregoing, according  
to the present invention the following advantages are  
20 obtainable. A first advantage is that it is possible to  
obtain correct average power level calculation. This is  
so because full power in the band of the channel under  
reception is involved in the calculation. A second  
advantage is that it is possible to obtain stable  
25 reception quality. This is so because the control timing  
is controlled based on the control amount. A third  
advantage is that it is possible to prevent erroneous  
power level measurement due to voltage rise shortage.



What is claimed is:

1. An AGC circuit in a CDMA receiver comprising an AGC loop for calculating received signal power level from a received signal and controlling the received signal power level to be constant, wherein:

the AGC loop includes means for controlling the control timing based on control amount.

2. A CDMA demodulator for receiving and demodulating a spread spectrum signal comprising an AGC loop including an intermediate frequency signal converter for converting the spread spectrum signal to an intermediate frequency signal and an AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage, wherein:

the AGC loop includes a power level calculating unit for calculating the level of full power in the band of a channel under reception.

3. A CDMA demodulator for receiving and demodulating a spread spectrum signal comprising an AGC loop including an intermediate frequency signal converter for converting the spread spectrum signal to an intermediate frequency signal and an AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage, wherein:

the AGC loop includes a power level calculating unit for calculating the level of full power in the band of a

channel under reception, the power level calculating unit starting the power level calculation from an instant corresponding to the forefront of a slot.

4. A CDMA demodulator for receiving and demodulating a spread spectrum signal comprising an AGC loop including an intermediate frequency signal converter for converting the spread spectrum signal to an intermediate frequency signal and an AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage, wherein:

the AGC loop includes a power level calculating unit for calculating the level of full power in the band of a channel under reception, the power level calculating unit starting the power level calculation from an instant corresponding to the forefront of a slot and making the length of the subject of calculation to be variable.

5. The CDMA demodulator according to claim 3 or 4, wherein the AGC loop further includes a control unit for calculating control time according to the result of calculation in the power level calculating unit, calculating and controlling the control timing based on control amount and feeding out the control voltage.

6. The CDMA demodulator according to claim 2, wherein the power level calculating unit starts the power level calculation from an intermediate part of slot.

7. A CDMA demodulator for receiving and demodulating a spread spectrum signal comprising:

an intermediate frequency signal converter for receiving the spread spectrum signal and converting the same signal to an intermediate frequency signal;

an AGC amplifier for variable gain amplifying the intermediate frequency signal with a control voltage;

a demodulating unit for demodulating the output signal of the AGC amplifier to a base-band signal;

a first low-pass filter for limiting the band of the base-band signal to a band corresponding to one channel and feeding out a first low-pass filter output signal;

an A/D converter for quantizing the level of full power in the band of the first low-pass filter output signal and feeding out the quantized signal;

a power level calculating unit for averaging the power level of the quantized signal for a predetermined period of time from an instant corresponding to the forefront of slot and feeding out an average power level signal representing the average power level;

a control unit for calculating control time based on the average power level represented by the average power level signal and feeding out control data upon reaching of a predetermined instant of time;

an A/D converter for converting the control data to an analog control signal; and

a second low-pass filter for waveform shaping the

along control signal and feeding the control voltage to the AGC amplifier.

8. A control timing controlling method adopted in an AGC circuit in a CDMA receiver comprising an AGC loop for computing a received signal power level from a received signal and controlling the received signal power level to be constant, wherein:

by taking the rise time of the next slot, the instant of start of control is variably set to be earlier than the forefront of the next slot so as to obtain coincidence of the instant of reaching of a desired voltage with the forefront of the next slot.

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ABSTRACT OF THE DISCLOSURE

A CDMA demodulator is disclosed, which comprises an AGC loop (13 to 20) including a IF signal converter (12) for converting a spread spectrum signal to an IF signal and an AGC amplifier (13) for variable gain  
5 amplifying the IF signal with a control voltage. The AGC loop also includes a power level calculating unit (17) for calculating the level of full power in the band of a channel under reception. Desirably, the power level  
10 calculating unit 17 starts the power level calculation from an instant corresponding to the forefront of slot. Desirably, the AGC loop further includes a control unit (18), which calculates control time based on the result of calculation in the power level calculating unit and  
15 feeds out a control voltage by calculating and controlling the control timing based on control amount. The power level calculating unit may start the power level calculation from an intermediate part of slot instead of the forefront thereof.

FIG. 1

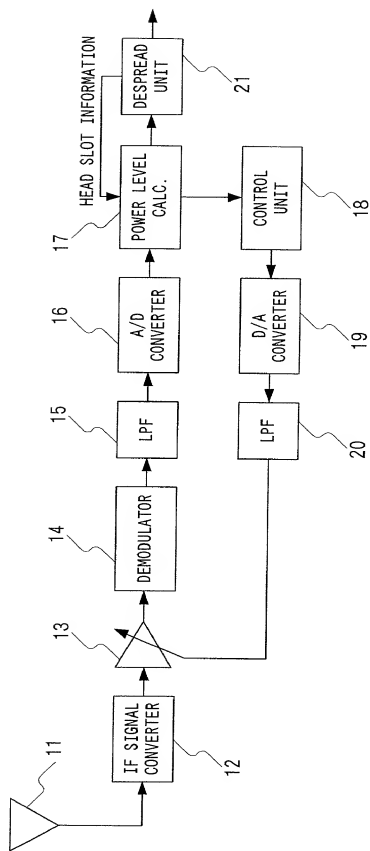


FIG.2

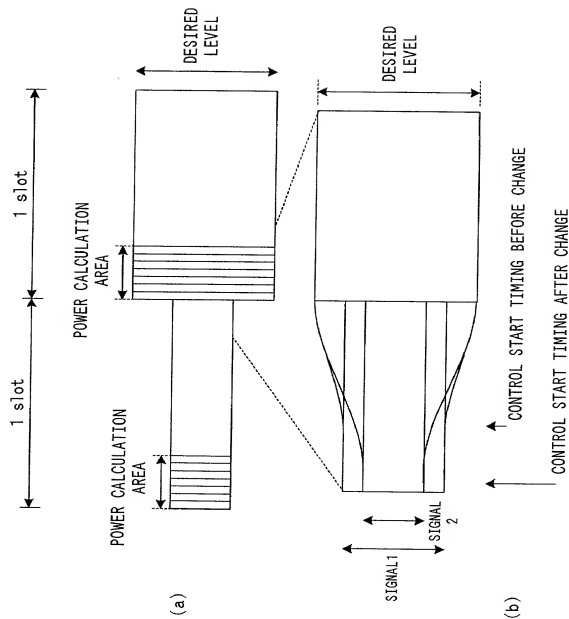


FIG.3

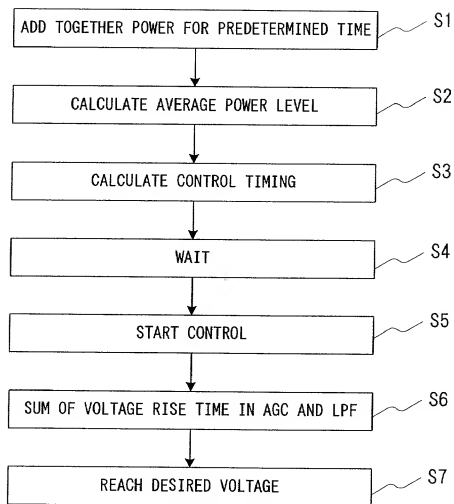


FIG.4

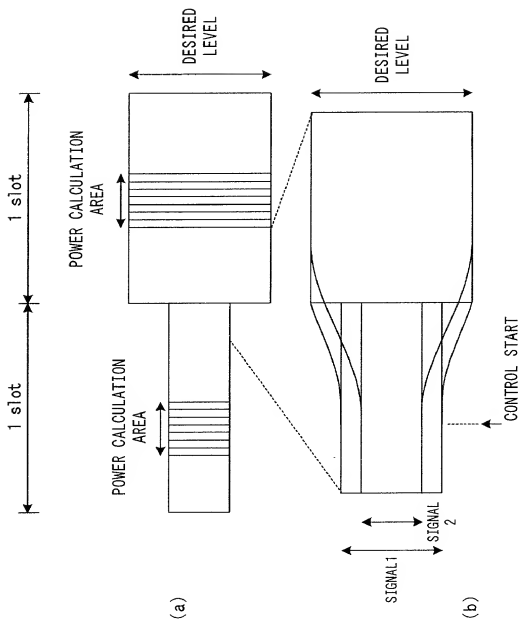
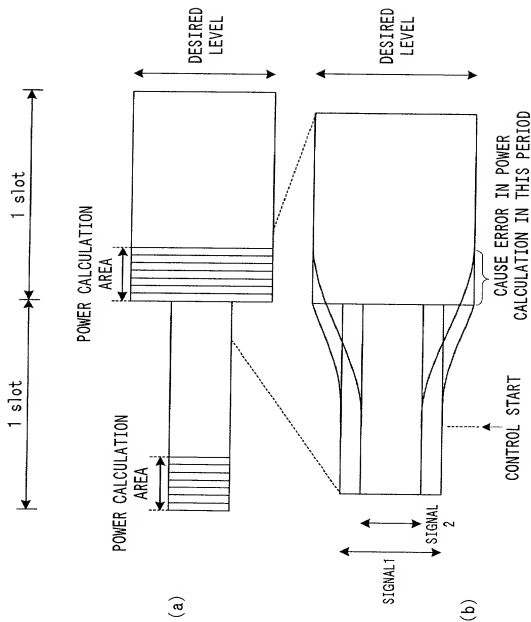


FIG.5



290301-1438

# Declaration and Power of Attorney for Patent Application

特許出願宣言書

## Japanese Language Declaration

私は、下欄に氏名を記載した発明として、以下の通り宣言する：

As a below named inventor, I hereby declare that.

私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、

My residence, post office address and citizenship are as stated below next to my name,

名所の発明に關し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一の発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の、最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CDMA RECEIVER AGC CIRCUIT

AND CDMA DEMODULATOR

その明細書を  
（該当するほうに印を付す）

the specification of which  
(check one)

☐ ここに添付する。

☒ is attached hereto.

☐ \_\_\_\_\_ 日に出願番号

☐ was filed on \_\_\_\_\_ as

第 \_\_\_\_\_ 号として提出し、

Application Serial No. \_\_\_\_\_

\_\_\_\_\_ 日に補正した。  
（該当する場合）

and was amended on \_\_\_\_\_  
(if applicable)

私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37部第1章第56条(a)項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

# Japanese Language Declaration

私は、合衆国法典第35部第119条、第172条、又は第365条に基づく下記の外国特許出願又は発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願又は発明者証出願を以下に明記する：

## Prior foreign applications 先の外国出願

290925/1999

JAPAN

13/10/1999

(Number)  
(番号)

(Country)  
(国名)

(Day/Month/Year Filed)  
(出願の年月日)

Priority claimed  
優先権の主張

☒

Yes  
あり

☐

No  
なし

(Number)  
(番号)

(Country)  
(国名)

(Day/Month/Year Filed)  
(出願の年月日)

☐

Yes  
あり

☐

No  
なし

(Number)  
(番号)

(Country)  
(国名)

(Day/Month/Year Filed)  
(出願の年月日)

☐

Yes  
あり

☐

No  
なし

(Number)  
(番号)

(Country)  
(国名)

(Day/Month/Year Filed)  
(出願の年月日)

☐

Yes  
あり

☐

No  
なし

(Number)  
(番号)

(Country)  
(国名)

(Day/Month/Year Filed)  
(出願の年月日)

☐

Yes  
あり

☐

No  
なし

私は、合衆国法典第35部第120条に基づき下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第35部第112条第1項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日又はPCT国際出願日の間に公表された進捗規則法典第37部第1章第56条(a)項に記載の所要の情報を開示すべき義務を有することを認める。

I hereby claim the benefit of Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose any material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)  
(出願番号)

(Filing Date)  
(出願日)

(現況)  
特許済み、保真中、放棄済み

(Status)

(patented, pending abandoned)

(Application Serial No.)  
(出願番号)

(Filing Date)  
(出願日)

(現況)  
特許済み、保真中、放棄済み

(Status)

(patented, pending abandoned)

私は、ここに自己の知識に基づいて行った陳述がすべて真実であり、自己の所有する情報及び得るところに従って行った陳述が真実であるとし、更に故意に虚偽の陳述等を行った場合、合衆国法典第18部第1001条により、罰金もしくは禁錮による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損なうことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true; and further that all statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

# Japanese Language Declaration

委任状: 私は、下記発明者として、以下の代理人をここに  
 選任し、本願の手続きを遂行すること並びにこれに関する一  
 切の行為を特許商標局に対して行うことを委任する。  
 (代理人氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby  
 appoint the following attorney(s) and/or agent(s) to  
 prosecute this application and transact all business in the  
 Patent and Trademark Office connected therewith (*list  
 name and registration number*)

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292;  
 Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg.  
 No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorro, Reg. No. 19,093;  
 Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No.  
 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710;  
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 Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William  
 H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778; Abraham J. Rosner, Reg.  
 No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; and Brett S. Sylvester, Reg. No. 32,765, my  
 attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and  
 request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, PLLC, 2100  
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第二の共同発明者の氏名 (該当する場合)	Full name of second joint inventor, if any	
同第二発明者の署名	日付	Second inventor's signature Date
住所	Residence	
国籍	Citizenship	
郵便の宛先	Post office address	

(第三又はそれ以降の共同発明者に対して同様な情報  
 および署名を提供すること。)

(Supply similar information and signature for third and  
 subsequent joint inventors)